VHDL LANGUAGE ELEMENTS
Reserved words

ABS	FOR	PACKAGE
ACCESS	FUNCTION	PORT
AFTER	GENERATE	PROCEDURE
ALIAS	GENERIC	PROCESS
ALL	GUARDED	RANGE
AND	IF	RECORD
ARCHITECTURE	IN	REGISTER
ARRAY	INOUT	REM
ASSERT	IS	REPORT
ATTRIBUTE	LABEL	RETURN
BEGIN	LIBRARY	SELECT
BLOCK	LINKAGE	SEVERITY
BODY	LOOP	SIGNAL
BUFFER	MAP	SUBTYPE
BUS	MOD	THEN
CASE	NAND	TO
COMPONENT	NEW	TRANSPORT
CONFIGURATION	NEXT	TYPE
CONSTANT	NOR	UNITS
DISCONNECT	NOT	UNTIL
DOWNTO	NULL	USE
ELSE	OF	VARIABLE
ELSIF	ON	WAIT
END	OPEN	WHEN
ENTITY	OR	WHILE
EXIT	OTHERS	WITH
FILE	OUT	XOR

VHDL LANGUAGE ELEMENTS

Identifiers

- An identifier is the name of an object
- Objects are named entities that can be assigned a value & have a specific data type
- Objects include signals, variables, & constants
- Must start with an alphabet character & end with an alphabet or a numeric character
- Can contain numeric characters or underscore & cannot contain spaces
- Are not case sensitive
- May be up to 32 characters long
- Cannot contain any reserved words

Symbols

--	begins comment (to end-of-line)
( )	encloses port names in entity declaration, enclose highest priority operations in Boolean & arithmetic expressions
' '	encloses scalar values
" "	encloses array values
;	ends VHDL statements & declarations
,	separates objects
:	separates object identifier names from mode & data type in declarations
<=	assigns values in signal assignment statements
:=	assigns values in variable assignment statements or to constants
=>	separates signal assignment statements from WHEN clause in CASE statements
+	addition operator
-	subtraction operator
=	equality operator
/=	inequality operator
>	greater than comparator
>=	greater than or equal to comparator
<	less than comparator
<=	less than or equal to comparator
&	concatenation operator

Synthesis Data Types

BIT	object can only have single-bit values of '0' or '1'
STD_LOGIC	object with multi-value logic including '0', '1', 'X', 'Z'
INTEGER	objects with whole number (decimal) values, e.g. 54, -21
BIT_VECTOR	objects with arrays of bits such as "10010110"
STD_LOGIC_VECTOR	objects with arrays of multi-value logic, eg. "01101XX"